CAL POLY POMONA DR. RAFI
ECE Dept.
LAB# 13

ECE 2300L

Prelab: Write a Verilog description using behavioral modeling for a counter to count in the sequence 0, 2, 3, 5, 6, 7, and repeat the sequence. Use T-flip-flops.

LAB: Compile the Verilog code. Write a simulation test bench to simulate the decoder

POSTLAB:

1. Write a Verilog description for a D flip-flop obtained using a JK flip-flop. Use behavioral modeling.

2. Write a Verilog description for a BCD adder for adding two single BCD digits. Use hierarchical modeling.