CAL POLY POMONA DR. RAFI

ECE Dept.

LAB# 12

ECE 2300L

Prelab:

Write a Verilog description for a 3-to-8 decoder with one HIGH enable. Use structural modeling.

LAB:

Compile the Verilog code. Write a simulation test bench to simulate the decoder

POSTLAB:

1. What does Verilog stand for?
2. What is the basic difference between C and Verilog.
3. What is meant by hierarchical modeling?
4. Write a Verilog description for a 4-bit binary adder. Use hierarchical modeling.