Cal Poly Pomona
ECE Dept.
ECE 2300L Lab # 11

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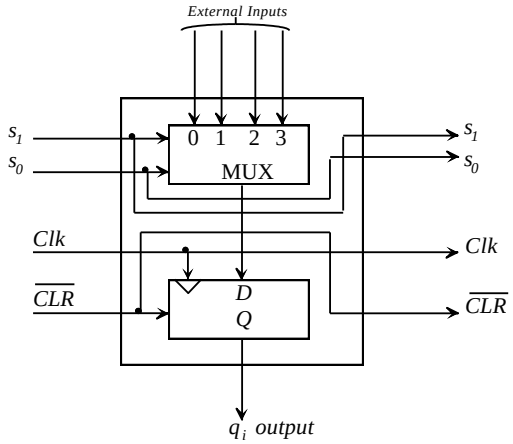
Prelab

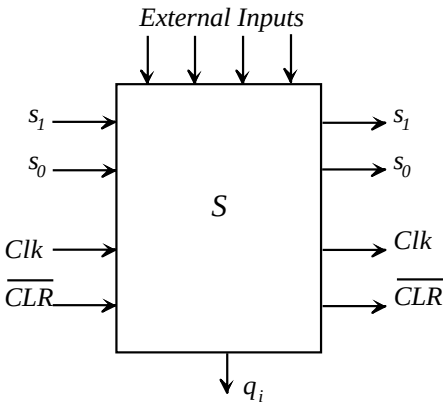
Design a 4-bit general-purpose register as follows:

S_1	S_0	Function
0	0	Load external data
0	1	Rotate left; ($A_0 \leftarrow A_3$, $A_i \leftarrow A_{i-1}$ for i = 1,2,3)
1	0	Rotate right; ($A_3 \leftarrow A_0$, $A_i \leftarrow A_{i+1}$ for i = 0,1,2)
1	1	Increment

Use the following cell *S* as the building block:



Internal Organization of the Basic Cell *S*



Block Diagram of the Basic Cell *S*

LAB:

Implement the above design and demonstrate to the instructor.

POSTLAB:

Design a 4-bit register with a reset input, a parallel input and a positive edge-triggered clock. The 4-bit register is cleared to 0 at the positive edge of the reset. On the other hand, if the load input is high, 4-bit data is transferred to the register at the positive edge of the clock.