Cal Poly Pomona<br>ECE Dept.<br>LAB \# 5<br>DR. Rafi

## Prelab

1. Design a $4 \times 16$ decoder using a minimum number of 74138 and logic gates.
2. Design a logic sing a minimum of 74138s ( $3 \times 8$ decoders) to generate the minterms $\mathrm{m}_{1}, \mathrm{~m}_{5}$ and $\mathrm{m}_{9}$ based on the four switch inputs S3, S2,S1, S0. Then display the selected minterm numbers (1 or 5 or 9 ) on a seven segment display by generating a 4-bit input ( $\mathrm{W}, \mathrm{X}, \mathrm{Y}, \mathrm{Z}$ ) for a BCD to seven-segment code converter. Turn an LED ON for all other minterms and blank the seven-segment display.

Note that these four inputs (W,X,Y,Z) can be obtained from the selected output line ( 1 or 5 or 9 ) of the decoders that is generated by the four input switches (S3, S2, S1, S0). Use a minimum number of logic gates. Determine the truth table, and then draw a logic diagram.

## LAB

Parts List: DIP switches, 74LS138 decoders (Two), One 74LS08, One 74LS32, One 74LS04, One 74LS47, seven-segment display, 1K \& 330 Ohms.

Implement the above circuit using a minimum number of decoder and gates. Demonstrate the operations using switches and LED, Seven segments display (select from Data book) etc. as needed. Postlab

Design a combinational circuit to generate the following:

$$
\begin{aligned}
& F_{0}=\operatorname{SUM}(m(1,3,4)) \\
& F_{1}=\operatorname{SUM}(m(0,2,4,7)) \\
& F_{2}=\operatorname{SUM}(m(0,1,3,5,6)) \\
& F_{3}=\operatorname{SUM}(m(2,6))
\end{aligned}
$$

Draw a logic diagram using a 74138 decoder and external gates.

